TILE-Gx™ 8000 Series Processor

High-Speed Networking

KEY APPLICATIONS

Network Infrastructure

- Routers (SMB, enterprise, core)
- Services blades (security offload, media services)

Network Security

- Firewall (SPI, proxy)
- VPN appliances (IPsec, SSL)
- Intrusion detection and prevention (IDS/IPS)
- Data leakage prevention (DLP)

Network Optimization

- WAN optimizer (compression, data caching, de-duplication)
- Server load balancer (SLB)
- Network monitoring (flow tracking and deep packet inspection)

Other:

- Data Forensics and e-Discovery (Live Data Capture and Correlation)
- Network Test Equipment (Wire-speed Packet Analysis & Generation)

Optimized for Networking Applications

The TILE-Gx™ 8000 series offers high performance for both control plane and data plane processing making it ideal for high speed packet processing and line rate security applications. TileDirect™ technology provides coherent I/O directly into the tile caches to deliver ultimate low-latency packet processing performance. The extensive I/O options make getting data in to and out of the system a matter of preference, not a compromise due to system limitations.

Flexible SERDES options include:

- XAUI
- SGMII
- Interlaken
- PCIe Gen2
- StreamIO

Most Scalable Processor Family

The TILE-Gx family is the most scalable processor in the industry with 16 to 100 cores on a single device. All four processors are software compatible allowing for easy deployment throughout an entire product matrix reducing time to market by simplifying development and leveraging existing code. The TILE-Gx is backward compatible with software developed for the TILE*Pro*™ family making for an easy migration path to adopt the latest features and performance enhancements.

Best Performance Per Watt

The TILE-Gx family combines Tilera's patented iMesh™ technology with the Tile Architecture™ to deliver the most efficient and high powered processor available. Low latency and high bandwidth interconnects ensure the 64-bit cores are able to maximize their performance and minimize system bottle necks. This efficiency allows each processor to run at lower clock speeds, saving power, yet still deliver the performance demanded by high speed networking applications.

	Features	Enables
Massively Scalable Performance	16 to 100 general purpose processor cores (tiles) 64-bit VLIW cores with 64-bit instruction bundle Up to 750 billion 32-bit operations per second (BOPS)	40 to 80 Gbps of Snort® IPS scanning 60 to 80 Gbps nProbe 64+ channels of OFDM baseband processing
Power Efficiency	1.0 to 1.5 GHz operating frequency 10 to 55 W for typical applications Idle tiles can be put into low-power sleep mode	Highest performance per watt Simple thermal management Small system form factor
Integrated Solution	Four 64-bit DDR3 memory controllers (optional ECC) Up to eight 10 GbE XAUI interfaces and two Interlaken interfaces Three Gen2 PCIe interfaces, each selectable as endpoint or root complex Wire-speed mPIPE™ packet processing engine	Reduces BOM cost – standard interfaces on-chip Dramatically reduced board real estate Up to 96 Gbps of PCIe bandwidth Over 80 Gbps of packet I/O bandwidth Up to 80 Gbps VPN performance
Multicore Development Environment Options	ANSI standard C/C++ compiler Advanced profiling and debugging designed for multicore programming Supports SMP Linux with 2.6	Run off-the-shelf C/C++ programs Reduces debug and optimization time Faster time-to-production code Standard multicore communication mechanisms

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Integrated Solution

The Tile architecture integrates a complete set of memory and I/O controllers, eliminating the need for an external north bridge or south bridge. This integration dramatically reduces the amount of board space required allowing for smaller form factors. It eliminates discrete components which reduces BOM costs and design complexity to lower system costs and speed time to market.

Standard Software Tools

Tilera's Multicore Development Environment™ (MDE) is a complete standards-based multicore programming solution that enables developers to take full advantage of the parallel processing potential of the Tile architecture.

The MDE leverages Open Source software and the developer's existing software code base to achieve impressive results in an extremely short period of time. As developers become more familiar with large-scale multicore, they can take advantage of enhanced tools and libraries offered in the MDE.

Tilera's MDE includes:

- Standard Eclipse-based IDE
- GCC compiler (ANSI C/C++)
- Multi-tile, timing-accurate simulator
- Whole chip debug and performance analysis
- Line-by-line profiling
- Full SMP Linux support
- TMC libraries for efficient inter-communication

	TILE-Gx8016	TILE-Gx8036	TILE-Gx8064	TILE-Gx8100
Core Count				
General Purpose Cores	16	36	64	100
I/O Features				
PCIe Gen2 ports	Two x4, One x2	One x8, Two x4	Two x8, One x4	Two x8, One x4
XAUI/Double XAUI Ports (max)	2/2	4/4	6/6	8/8
Interlaken Ports (50 Gb)	0	0	2	2
SGMII Ports (10/100/1000)	12	16	24	32
mPIPE Throughput	30 Mpps	60 Mpps	90 Mpps	120 Mpps
USB Ports	2	2	3	3
Memory Features				
Total cache	5 MBytes	12 MBytes	20 MBytes	32 MBytes
# Memory Controllers	2	2	4	4
Max DDR3 Speed	1600	1866	2133	2133
MiCA Acceleration				
Symmetric Crypto	20 Gbps AES	40 Gbps AES	60 Gbps AES	80 Gbps AES
PubKey Crypto	15K RSA/sec	30K RSA/sec	45K RSA/sec	60K RSA/sec
Compress/Decompress	5 Gbps	10 Gbps	15 Gbps	20 Gbps

www.tilera.com/tile-gx8000

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